IN THE CLAIMS:

Please amend the claims to read as follows:

1. (Currently Amended) A semiconductor package, comprising:

a die;

a wire bonding package substrate positioned under the die, the package substrate having a die attach pad and a plurality of lead fingers surrounding the die attach pad;

a plurality of wire bonds electrically connecting the die to the plurality of lead fingers;

a bottom plate positioned under the die attach pad; and

an insulator set between the die attach pad and the bottom plate such that the die attach pad and the bottom plate are electrically insulated from each other by the insulator; wherein at least one of the bottom plate and the insulator has at least one expansion slot.

2. (Original) The semiconductor package of claim 1, wherein the package substrate includes a tie bar connected to the die attach pad.

3. (Original) The semiconductor package of claim 1, further comprising:

a molding cap covering at least a portion of the die, package substrate, wire bonds, insulator, and bottom plate.

4. (Original) The semiconductor package of claim 1, wherein the die attach pad is larger than the die such that a portion of the die attach pad is exposed around the die.

5. (Original) The semiconductor package of claim 4, wherein the bottom plate is larger than the die attach pad such that a portion of the bottom plate is exposed around the die attach pad.

6. (Original) The semiconductor package of claim 5, wherein the plurality of wire bonds electrically connects to the exposed portion of the die attach pad.

7. (Original) The semiconductor package of claim 6, wherein the plurality of wire bonds electrically connects to the exposed portion of the bottom plate.

8. (Original) The semiconductor package of claim 5, wherein the exposed portion of the bottom plate has an alignment structure for aligning the bottom plate with the die attach pad.

9. (Original) The semiconductor package of claim 8, wherein the alignment structure is an up-set flange.

10. (Original) The semiconductor package of claim 9, wherein the up-set flange has a surface leveled with the die attach pad.

11. (Original) The semiconductor package of claim 8, wherein the alignment structure is an edge of the bottom plate.

12. (Original) The semiconductor package of claim 8, wherein the alignment structure is a dowel hole.

13. (Original) The semiconductor package of claim 1, wherein the insulator and the bottom plate have matching expansion slots.

14. (Original) The semiconductor package of claim 1, wherein the die attach pad has an expansion slot.

15. (Original) The semiconductor package of claim 1, wherein the insulator is selected from the group consisting of a non-conductive adhesive tape and a non-conductive adhesive liquid.

16. (Original) The semiconductor package of claim 1, wherein the die is attached to the die attach pad with a die attach epoxy.

17. (Original) The semiconductor package of claim 1, wherein the die attach pad is connected to a ground source of the semiconductor package and the bottom plate is connected to a power source of the semiconductor package.

18. (Currently Amended) A method of assembling a semiconductor package, comprising:

providing a wire bonding package substrate with a die attach pad and a plurality of lead forgers surrounding the die attach pad, the die attach pad having a top surface and a bottom surface;

attaching a die to the top surface of the die attach pad;

setting in place an insulator to a bottom plate;

attaching the bottom plate to the bottom surface of the die attach pad such that the bottom plate and the die attach pad are electrically insulated from each other by the insulator; ~~and~~

electrically connecting a plurality of wire bonds from the die to the plurality of lead fingers; and

providing at least one expansion slot within at least one of the bottom plate and the insulator.

19. (Original) The method of claim 18, further comprising:

forming a molding cap covering at least a portion of the die, package substrate, wire bonds, insulator, and bottom plate.

20. (Original) The method of claim 18, wherein the die attach pad is larger than the die such that a portion of the die attach pad is exposed around the die.

21. (Original) The method of claim 20, wherein the bottom plate is larger than the die attach pad such that a portion of the bottom plate is exposed around the die attach pad.

22. (Original) The method of claim 21, further comprising:

electrically connecting the plurality of wire bonds to the exposed portion of the die attach pad.

23. (Original) The method of claim 22, further comprising:

electrically connecting the plurality of wire bonds to the exposed portion of the bottom plate.

24. (Original) The method of claim 21, wherein attaching the bottom plate to the bottom surface of the die attach pad includes aligning the bottom plate with the die attach pad with an alignment structure that is integrated with the exposed portion of the bottom plate.

25. (Original) The method of claim 24, wherein the alignment structure is an up-set flange.

26. (Original) The method of claim 25, wherein the up-set flange has a surface leveled with the top surface of the die attach pad.

27. (Original) The method of claim 24, wherein the alignment structure is an edge of the bottom plate.

28. (Original) The method of claim 24, wherein the alignment structure is a dowel hole.

29. (Original) The method of claim 18, wherein the insulator and the bottom plate have matching expansion slots.

30. (Original) The method of claim 18, wherein the die attach pad has an expansion slot.

31. (Original) The method of claim 18, wherein the insulator is selected from the group consisting of a non-conductive adhesive tape and a non-conductive adhesive liquid.

32. (Original) The method of claim 18, wherein the die is attached to the die attach pad with a die attach epoxy.

33. (Original) The method of claim 18, wherein the die attach pad is connected to a ground source of the semiconductor package and the bottom plate is connected to a power source of the semiconductor package.

34. (Currently Amended) A semiconductor package, comprising:

a die;

a wire bonding package substrate positioned under the die, the package substrate having a die attach pad and a plurality of lead fingers surrounding the die attach pad;

a plurality of wire bonds electrically connecting the die to the plurality of lead fingers;

a bottom plate positioned under the die attach pad, wherein the bottom plate and the die attach pad have means for lowering inductance; and

an insulator set between the die attach pad and the bottom plate such that the die attach pad and the bottom plate are electrically insulated from each other by the insulator; wherein at least one of the bottom plate and the insulator has at least one expansion slot therein.

35. (New) A semiconductor package, comprising:

a die;

a wire bonding package substrate positioned under the die, the package substrate having a die attach pad and a plurality of lead fingers surrounding the die attach pad;

a plurality of wire bonds electrically connecting the die to the plurality of lead fingers;

a bottom plate positioned under the die attach pad; and

an insulator set between the die attach pad and the bottom plate such that the die attach pad and the bottom plate are electrically insulated from each other by the insulator,

wherein the die attach pad has an expansion slot.

36. (New) A method of assembling a semiconductor package, comprising:

providing a wire bonding package substrate with a die attach pad and a plurality of lead forgers surrounding the die attach pad, the die attach pad having a top surface and a bottom surface;

attaching a die to the top surface of the die attach pad;

setting in place an insulator to a bottom plate;

attaching the bottom plate to the bottom surface of the die attach pad such that the bottom plate and the die attach pad are electrically insulated from each other by the insulator; and

electrically connecting a plurality of wire bonds from the die to the plurality of lead fingers,

wherein the die attach pad has an expansion slot.